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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/805,227	03/22/2004	Osamu Hirabayashi	250848US2S	9121
22850	7590	03/14/2006	EXAMINER	
OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C. 1940 DUKE STREET ALEXANDRIA, VA 22314			RADOSEVICH, STEVEN D	
		ART UNIT	PAPER NUMBER	
			2138	

DATE MAILED: 03/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/805,227	HIRABAYASHI, OSAMU
	Examiner	Art Unit
	Steven D. Radosevich	2138

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 22 March 2004.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-20 is/are pending in the application.
 - 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-20 is/are rejected.
- 7) Claim(s) 20 is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 22 March 2004 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 - Certified copies of the priority documents have been received in Application No. _____.
 - Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>3/22/04</u> | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claims 1-20 are present for examination.

Priority

Acknowledgement is made that foreign priority either or domestic is claimed for this application and as such the filing date (10/20/2003) is being used for this examination.

Information Disclosure Statement

Acknowledgement is made that no Information Disclosure Statement (IDS) was provided with the application.

Drawings

The drawings are not objected and as such are accepted.

Claim Objections

Claim 20 is objected to because it is believed to be improperly dependent on claim 12, which is not a test method. For the purposes of this examination claim 20, which is a test method claim will be treated as being dependent on claim 13, which is the independent claim that first introduces a test method. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 12 recites the limitation "semiconductor chip" in the first line or preamble of the claim. There is insufficient antecedent basis for this limitation in the claim. For the

purposes of this examination it will be assumed that "the semiconductor chip" was intended to be "the semiconductor integrated circuit" that is present in claim 10 and on which claim 12 is dependent. Appropriate correction is required to overcome this 112 rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sharma (6910169), Giles et al. (4680760), and further in view of Matsuda et al. (5509132).

1. As per claim 1, Sharma teaches a semiconductor integrated circuit comprising:
 - A memory (wires column 4 line 31);
 - An ECC circuit that has an error correction function of N (N is a natural number) bits for output data of the memory (column 5 lines 25-31).

Sharma does not explicitly teach the semiconductor integrated circuit comprising:

An error detection circuit configured to output a signal indicative of the following fact, if a total of an error bit number n_1 detected by the ECC circuit when a first data pattern in testing target addresses of the memory is read out and an error bit number n_2 detected by the ECC circuit when a second data pattern that is an inversion of the first data pattern in at least part of the testing target addresses is read out exceeds N.

However in an analogous art Giles teaches a memory (column 2 line 53) wherein a first data pattern in testing target addresses of the memory is read out with errors (MISS) observed each time one accrues and when a second data pattern that is an inversion of the first data pattern is read out of the memory with errors (MISS) observed each time one accrues (column 4 lines 9-21).

Therefore, one of ordinary skill in the art at the time the invention was made would have been motivated to combine the teachings of Giles and Sharma described above since Sharma states that Sharma's teaching does not detect offsetting multiple error (column 4 lines 18-24) while Giles indicates that all errors will be detected using his teachings (column 4 lines 41-42).

Giles and Sharma as combined above does not specifically teach outputting a signal indicative of when a total number of errors exceeds the error correction capability N of an ECC.

However in an analogous art Matsuda teaches outputting a signal indicative of when a total number of errors exceeds the error correction capability N of an ECC (column 9 lines 39-42).

Therefore, one of ordinary skill in the art at the time the invention was made would have been motivated to combine the teaches of Giles with Sharma with the teaches of Matsuda, to indicate when a total number of errors in a memory exceeds the error correction capability N of an ECC used in-order to indicate that the ECC is not appropriate or capable of achieving the desired results of correcting all errors since ECC can only be used successfully if the number of errors does not exceed the correction capability of the ECC.

2. As per claim 2, Giles teaches a BIST circuit configured to read the first data pattern out of the testing target addresses of the memory as a first operation, write the second pattern in at least a part of the testing target addresses as a second operation, and read out the written second data pattern (column 4 lines 9-21).
3. As per claim 3, Giles teaches wherein the BIST circuit repeats the first and second operations while changing the testing target addresses (column 4 lines 9-21).
4. As per claim 4, Giles teaches wherein the BIST circuit writes the first data pattern as background data in all the addresses of the memory before the first and second operations are repeated (column 4 lines 9-21).
5. As per claim 5, Matsuda and Giles as combined above teaches wherein:

The ECC circuit outputs SEC signals indicative of the error bit numbers n1 and n2 (Matsuda - column 8 lines 24-29, column 9 lines 39-42, column 11 lines 20-25, and figure 1);

The BIST circuit outputs a first reading signal during reading of the first data pattern, and a second reading signal during reading of the second data pattern (Giles - column 4 lines 9-21 and figure 1).

The error detection circuit stores the error bit number n1 upon reception of the first reading signal, and the error bit number n2 upon reception of the second reading signal, and calculates n1+n2 by logic processing (Matsuda - column 9 lines 39-42, column 11 lines 20-25, and figures 1 and 6).

6. As per claims 6 and 15, Matsuda and Giles as combined above teaches wherein the error bit numbers n1 and n2 are stored in registers (Matsuda - column 8 lines 24-30 and figure 6).

7. As per claims 7 and 16, Matsuda and Giles as combined above teaches wherein:

Only a bit among the bits of the testing target addresses in which the second data pattern has been written is set to be checked (Giles - column 4 lines 9-21);

The error bit number n2 is counted in for an error generated in the bit to be checked (Matsuda - column 8 lines 24-30).

8. As per claims 8 and 9, Matsuda, Giles, and Sharma as combined above teaches the testing target addresses contain data bits and code bits, and bits other than the bit to be checked are part of the data/code bits (Sharma - column 6 lines 12-16).

9. As per claim 10, Matsuda and Giles as combined above teaches wherein:

The ECC circuit outputs an SEC signal indicative of presence of an error to each of the bits of the testing target addresses (Matsuda - column 39-42);

The BIST circuit outputs a state signal indicative of the first and second test patterns (Giles - column 4 lines 9-21 and figure 1); and

The error detection circuit specifies the bit to be checked based on the state signal, and obtains the error bit number n2 for the bit to be checked based in the SEC signal (Giles – column 4 lines 9-21 and Matsuda – column 9 lines 39-42).

10. As per claim 11, Sharma teaches wherein the N is a 1 (column 5 lines 27-31).

11. As per claim 12, Matsuda and Giles as combined above teaches wherein the semiconductor integrated circuit constitutes a part of the system LSI (figure 1).

12. As per claim 13, Matsuda teaches a test method of a semiconductor memory with an ECC circuit comprising:

Detecting an error bit number n1 by using the ECC circuit that has an error correction function of N (N is a natural number) bits (column 8 lines 24-29, column 9 lines 53-54, and column 11 lines 20-25);

Detecting an error bit number n2 by using the ECC circuit (column 8 lines 24-29); and

Determining whether a total of the error bit numbers n1 and n2 exceeds N or not (column 8 lines 24-29).

Matsuda does not specifically teach:

Reading a first data pattern out of testing target addresses of a memory;
and

Writing/reading a second data pattern that is an inversion of the first data
pattern in at least a part of the testing target addresses.

However in an analogous art Giles teaches testing comprising:

Reading a first data pattern out of testing target addresses of a memory
(column 4 lines 9-21); and

Writing/reading a second data pattern that is an inversion of the first data
pattern in at least a part of the testing target addresses (column 4 lines 9-21).

Therefore, one of ordinary skill in the art at the time the invention was made
would have been motivated to combine the above teachings of Matsuda and Giles in-
order to as stated by Giles catch all stuck-at-faults (column 4 lines 41-42) and determine
correct-ability.

13. As per claim 14, Giles teaches wherein after the first data pattern is written as
background data in all the addresses of the memory, the reading of the first data pattern
and the writing/reading of the second data pattern are repeated while the testing target
addresses are changed (column 4 lines 9-21).

14. As per claim 17, Giles teaches determining the presence of an error for each of
the bits of the testing target addresses (column 4 lines 9-21).

15. As per claim 18, Giles teaches wherein the bit to be checked is specified based on
the first and second data patterns (column 4 lines 9-21).

16. As per claim 19, Giles teaches wherein the first and second data patterns are generated in a chip (column 3 lines 29-30 and column 4 lines 9-21).

17. As per claim 20, Matsuda teaches wherein the semiconductor integrated circuit is determined to be a defective product when a total of the error bit number n1 and n2 exceeds N (column 8 lines 24-29 and column 9 lines 39-41).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven D. Radosevich whose telephone number is 571-272-2745. The examiner can normally be reached on 9am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decay can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Steven D. Radosevich
Examiner
Art Unit 2138


GUY LAMARRE
PRIMARY EXAMINER